WHAT IS CLAIMED IS:

1. A method for forming short-channel transistors, the method comprising the steps of:

forming a first oxide layer and a sacrificial layer one after another on a semiconductor substrate and etching the sacrificial layer, thus forming a residual sacrificial layer pattern;

conducting an ion implantation using the residual sacrificial layer pattern as a mask, thus forming an LDD ion-implant layer in the semiconductor substrate;

forming the first spacers on both side walls of the residual sacrificial layer pattern;

conducting an ion implantation using the residual sacrificial layer pattern and the first spacers as a mask, thus forming a source/drain ion-implant layer under the LDD ion-implant layer;

forming a nitride layer and a second oxide layer one after another on the whole surface of the former resultant object and conducting an annealing treatment, thus forming source/drain regions;

conducting chemical-mechanical polishing (CMP) processes to the extent that an upper surface of the residual sacrificial

layer pattern is exposed, and removing the residual sacrificial layer pattern through etching;

forming the second spacers on side walls of a portion where the residual sacrificial layer patter is removed;

conducting an ion implantation on the substrate between the second spacers, thus forming a punch-stop ion implant layer;

etching the first oxide layer under the portion where the residual sacrificial layer pattern is removed, and forming a gate insulation layer; and

forming a gate on the portion where the residual sacrificial layer pattern is removed.

2. The method for forming short-channel transistors as claimed in claim 1, wherein upon etching the sacrificial layer, the first oxide layer is used as an etch stopper layer.

3. The method for forming short-channel transistors as claimed in claim 1, wherein the gate insulation layer and the gate are formed after the source/drain regions are previously formed.

4. The method for forming short-channel transistors as

claimed in claim 1, wherein the sacrificial layer is formed of polysilicon.

5. The method for forming short-channel transistors as claimed in claim 1, wherein the second oxide layer is multi-layered.

6. The method for forming short-channel transistors as claimed in claim 1, wherein the punch-stop ion implant layer is adapted as a threshold-voltage adjustment ion implant layer.

7. The method for forming short-channel transistors as claimed in claim 1, wherein upon ion implantation of LDD and the source/drain, the first oxide layer is used as a buffer layer for ion implantation.

8. The method for forming short-channel transistors as claimed in claim 1, wherein the first and second spacers are formed of the same materials.

9. The method for forming short-channel transistors as claimed in claim 1 or 8, wherein the first and second spacers are formed of nitride layers.